



# SCHOTTKY BIPOLAR LSI MICROCOMPUTER SET

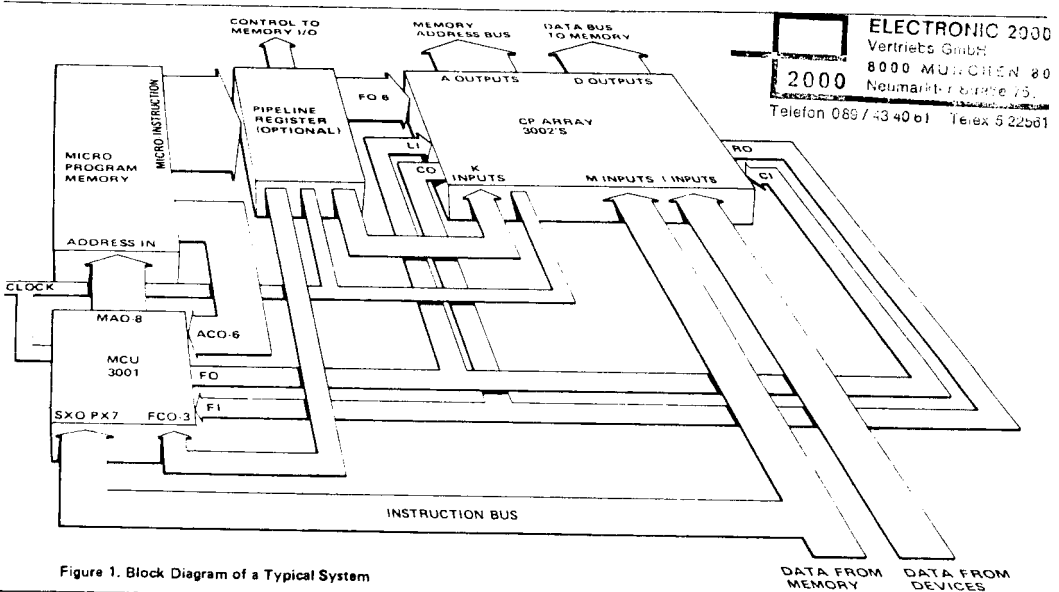
# 3002 *3002* CENTRAL PROCESSING ELEMENT

The INTEL<sup>®</sup> Bipolar Microcomputer Set is a family of Schottky bipolar LSI circuits which simplify the construction of microprogrammed central processors and device controllers. These processors and controllers are truly microprogrammed in the sense that their control logic is organized around a separate read-only memory called the microprogram memory. Control signals for the various processing elements are generated by the microinstructions contained in the microprogram memory. In the implementation of a typical central processor, as shown below, the microprogram interprets a higher level of instructions called macroinstructions, similar to those found in a small computer. For device controllers, the microprograms directly implement the required control functions.

The INTEL<sup>®</sup> 3002 Central Processing Element contains all of the circuits that represent a 2-bit wide slice through the data processing section of a digital computer. To construct a complete central processor for a given word width N, it is simply necessary to connect an array of N/2 CPE's together. When wired together in such an array, a set of CPE's provide the following capabilities:

- 2's complement arithmetic
- Logical AND, OR, NOT and exclusive-OR
- Incrementing and decrementing
- Shifting left or right
- Bit testing and zero detection
- Carry look-ahead generation
- Multiple data and address busses

- High Performance — 100 ns Cycle Time
- TTL and DTL Compatible
- N-Bit Word Expandable Multi-Bus Organization
  - 3 Input Data Buses
  - 2 Three-State Fully Buffered Output Data Buses
- 11 General Purpose Registers
- Full Function Accumulator
- Independent Memory Address Register
- Cascade Outputs for Full Carry Look-Ahead
- Versatile Functional Capability
  - 8 Function Groups
  - Over 40 Useful Functions
  - Zero Detect and Bit Test
- Single Clock
- 28 Pin DIP



**ELECTRONIC 2000**  
Vertriebs GmbH  
8000 MÜNCHEN 80  
Neumarktstraße 75.  
2000  
Telefon 089 / 43 40 61 Telex 5 22661

Figure 1. Block Diagram of a Typical System

Other members of the INTEL Bipolar Microcomputer Set:

3001 Microprogram Control Unit	3214 Priority Interrupt Control Unit	3304A Schottky Bipolar ROM (512 x 8)
3003 Look-Ahead Carry Generator	3226 Inverting Bi-Directional Bus Driver	3601 Schottky Bipolar PROM (256 x 4)
3212 Multi-Mode Latch Buffer	3301 Schottky Bipolar ROM (256 x 4)	3604 Schottky Bipolar PROM (512 x 8)

## PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE <sup>(1)</sup>
1, 2	I <sub>0</sub> -I <sub>1</sub>	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active LOW
3, 4	K <sub>0</sub> -K <sub>1</sub>	Mask Bus Inputs The mask bus inputs provide a separate input port for the microprogram memory, to allow mask or constant entry.	Active LOW
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the INTEL 3003 Look-Ahead Carry Generator.	
7	CO	Ripply Carry Output The ripple carry output is only disabled during shift right operations.	Active LOW Three-state
8	RO	Shift Right Output The shift right output is only enabled during shift right operations.	Active LOW Three-state
9	LI	Shift Right Input	Active LOW
10	CI	Carry Input	Active LOW
11	EA	Memory Address Enable Input When in the LOW state, the memory address enable input enables the memory address outputs (A <sub>0</sub> -A <sub>1</sub> ).	Active LOW
12-13	A <sub>0</sub> -A <sub>1</sub>	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active LOW Three-state
14	GND	Ground	
15-17, 24-27,	F <sub>0</sub> -F <sub>6</sub>	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	
18	CLK	Clock Input	
19-20	D <sub>0</sub> -D <sub>1</sub>	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active LOW Three-state
21-22	M <sub>0</sub> -M <sub>1</sub>	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active LOW
23	ED	Memory Data Enable Input When in the LOW state, the memory data enable input enables the memory data outputs (D <sub>0</sub> -D <sub>1</sub> )	Active LOW
28	V <sub>CC</sub>	+5 Volt Supply	

### NOTE:

1. Active HIGH, unless otherwise specified.

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