



SCHOTTKY BIPOLAR LSI MICROCOMPUTER SET

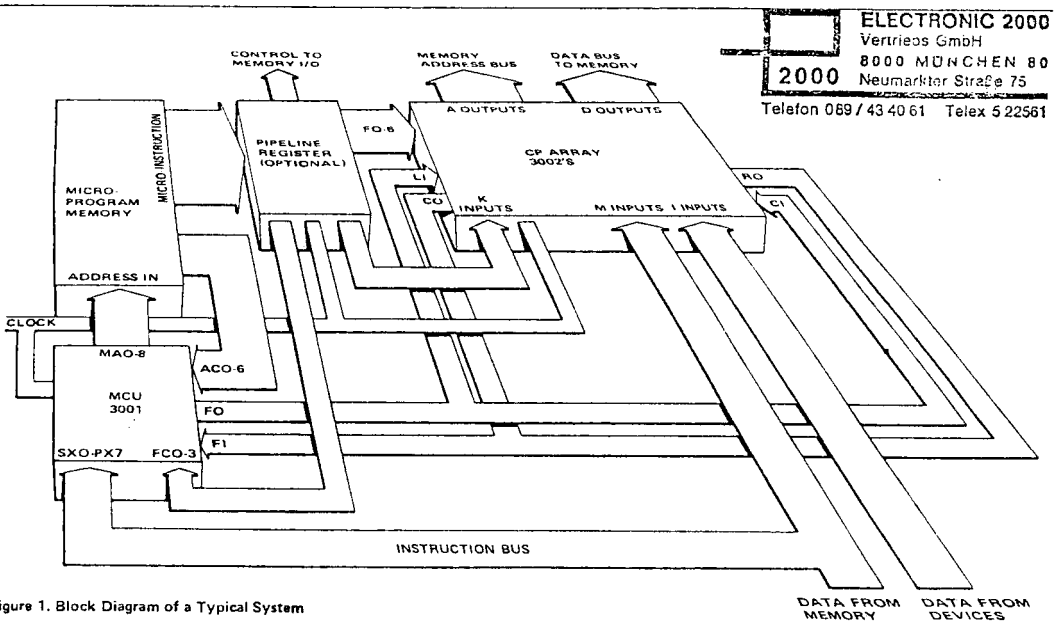
3001 MICROPROGRAM CONTROL UNIT

The INTEL Bipolar Microcomputer Set is a family of Schottky bipolar LSI circuits which simplify the construction of microprogrammed central processors and device controllers. These processors and controllers are truly microprogrammed in the sense that their control logic is organized around a separate read-only memory called the microprogram memory. Control signals for the various processing elements are generated by the microinstructions contained in the microprogram memory. In the implementation of a typical central processor, as shown below, the microprogram interprets a higher level of instructions called macroinstructions, similar to those found in a small computer. For device controllers, the microprograms directly implement the required control functions.

The INTEL 3001 Microprogram Control Unit (MCU) controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

- Maintenance of the microprogram address register.
- Selection of the next microinstruction based on the contents of the microprogram address register.
- Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence.
- Saving and testing of carry output data from the central processor (CP) array.
- Control of carry/shift input data to the CP array.
- Control of microprogram interrupts.

- High Performance — 85 ns Cycle Time
- TTL and DTL Compatible
- Fully Buffered Three-State and Open Collector Outputs
- Direct Addressing of Standard Bipolar PROM or ROM
- 512 Microinstruction Addressability
- Advanced Organization
 - 9-Bit Microprogram Address Register and Bus
 - 4-Bit Program Latch
 - Two Flag Registers
- Eleven Address Control Functions
 - Three Jump and Test Latch Functions
 - 16-way Jump and Test Instruction Bus Function
- Eight Flag Control Functions
 - Four Flag Input Functions
 - Four Flag Output Functions
- 40 Pin DIP



ELECTRONIC 2000
Vertriebs GmbH
8000 MÜNCHEN 80
Neumarkter Straße 75
Telefon 069 / 43 40 61 Telex 5 22561

Figure 1. Block Diagram of a Typical System

Other members of the INTEL Bipolar Microcomputer Set:

- | | | |
|---------------------------------|--|--------------------------------------|
| 3002 Central Processing Element | 3214 Priority Interrupt Control Unit | 3304A Schottky Bipolar ROM (512 x 8) |
| 3003 Look-Ahead Carry Generator | 3226 Inverting Bi-Directional Bus Driver | 3601 Schottky Bipolar PROM (256 x 4) |
| 3212 Multi-Mode Latch Buffer | 3301 Schottky Bipolar ROM (256 x 4) | 3604 Schottky Bipolar PROM (512 x 8) |

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE ⁽¹⁾
1-4	PX ₄ -PX ₇	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	active LOW
5, 6, 8, 10	SX ₀ -SX ₃	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	active LOW
7, 9, 11	PR ₀ -PR ₂	PR-Latch Outputs The PR-latch outputs are asynchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	open collector
12, 13, 15, 16	FC ₀ -FC ₃	Flag Logic Control Inputs The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	
14	FO	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	active LOW three-state
17	FI	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: the flag input data is saved in the F-latch when the clock input (CLK) is low.	active LOW
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description, page 6). It can be used to provide the strobe signal required by the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits.	
19	CLK	Clock Input	
20	GND	Ground	
21-24 37-39	AC ₀ -AC ₆	Next Address Control Function Inputs All jump functions are selected by these control lines.	
25	EN	Enable Input When in the HIGH state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26-29	MA ₀ -MA ₃	Microprogram Column Address Outputs	three-state
30-34	MA ₄ -MA ₈	Microprogram Row Address Outputs	three-state
35	ERA	Enable Row Address Input When in the LOW state, the enable row address input independently disables the microprogram row address outputs. It can be used with the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits to facilitate the implementation of priority interrupt systems.	
36	LD	Microprogram Address Load Input When in the active HIGH state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction busses into the microprogram register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	
40	VCC	+5 Volt Supply	

NOTE:

(1) Active HIGH unless otherwise specified.